Integrated Back to Back Barrier-N-N$^+$ Varactor Diode Tripler Using a Split-Waveguide Block

Debabani Choudhury, *Member, IEEE*, Peter H. Siegel, *Member, IEEE*, R. Peter Smith, Antti V. Räisänen, *Fellow, IEEE*, Suzanne C. Martin, and Margaret A. Frerking, *Member, IEEE*

***Abstract*— The back-to-back barrier-N-N$^+$ (bbBNN) varactor is a nonlinear device being developed for frequency multiplier applications above 100 GHz. Its symmetrical C–V characteristic, low series resistance, freedom from external bias and suitability to planarization make it an ideal choice for high frequency, low power, odd harmonic generation. In this paper, the performance of a 220-GHz waveguide tripler using, for the first time, a planar GaAs bbBNN device integrated on a quartz microstrip circuit is presented. A new split-waveguide block design has been employed to provide the proper embedding impedances to the device at the input and third harmonic output frequencies. A flange-to-flange tripling efficiency of 7% has been obtained at 220 GHz with an output power in excess of 700 μW. This is believed to be the highest conversion efficiency yet reported for a tripler with an integrated device at this frequency. Theoretical calculations indicate that substantial improvement is possible with modest changes to the device and circuit parameters.**

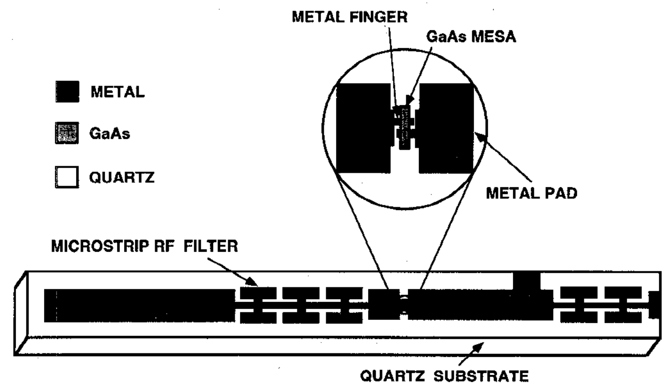


Fig. 1. Schematic of a planar bbBNN varactor integrated with the microstrip filter structure on a fused quartz substrate.

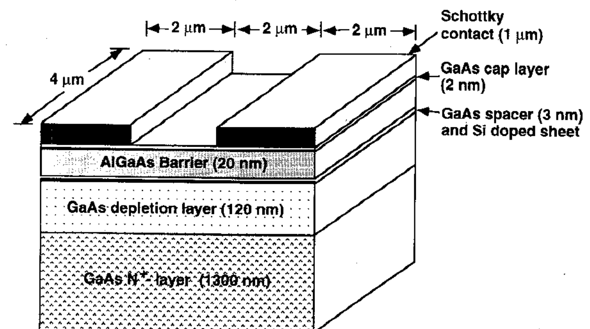


Fig. 2. Semiconductor layer structure of the bbBNN device.

I. Introduction

SPACE-BASED local oscillator sources for heterodyne radiometry at millimeter and submillimeter wavelengths favor low power consuming, mechanically robust, solid-state devices which can operate at ambient temperatures around 300°K. The most common approach uses solid-state harmonic generators, such as whisker-contacted varactor diode frequency multipliers, pumped by millimeter-wave fundamental sources, typically Gunn diode oscillators up to 140 GHz. Although the whisker contacted Schottky varactor diodes have proven very effective, there remains great interest in developing more robust, planar device technologies which are capable of operating well into the submillimeter wavelength range and have the potential to deliver sufficient amounts of power for both astrophysics and Earth remote sensing receiver applications.

The back-to-back barrier-N-N$^+$ (bbBNN) varactor diode is one such candidate for THz frequency space applications [1]–[3]. The sharp C–V characteristic of this device, which is peaked around zero volts, allows for potentially high multiplication efficiency at low input power levels. This is an advantage, particularly at THz frequencies, where the available input power from prior multiplication stages necessarily will be quite low. In addition, its symmetric C–V characteristic offers significant benefits for odd harmonic multiplier applications since idler circuits at the even harmonics are not needed. Finally, the bbBNN device does not require external dc bias to operate at peak efficiency, minimizing the number of off-chip circuit connections. On the device side, the bbBNN offers significant processing advantages. There is no ohmic contact, thereby reducing a substantial parasitic series resistance contribution. The device exhibits very low leakage current (<10 nA), has low internal parasitic resistance (10–20 Ω at dc), high dynamic cutoff frequency (>1 THz), is easily planarized and can be arrayed in stacks to increase power handling capacity.

Manuscript revised November 17, 1994. This work was carried out at the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

D. Choudhury was with the Jet Propulsion Laboratory, California Institute of Technology, Pasedena, CA 91109 USA. She is now with Millitech Corp., South Deerfield, MA 01373 USA.

P. H. Siegel, R. P. Smith, S. C. Martin, and M. A. Frerking are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

A. V. Räisänen is with the Radio Laboratory, Helsinki University of Technology, FIN-02150 Espoo, Finland. He was on sabbatical leave at the Jet Propulsion Laboratory as a senior research fellow of the National Research Council, Helsinki University of Technology, Finland.

IEEE Log Number 9409123.

0018–9480/95$04.00 © 1995 IEEE

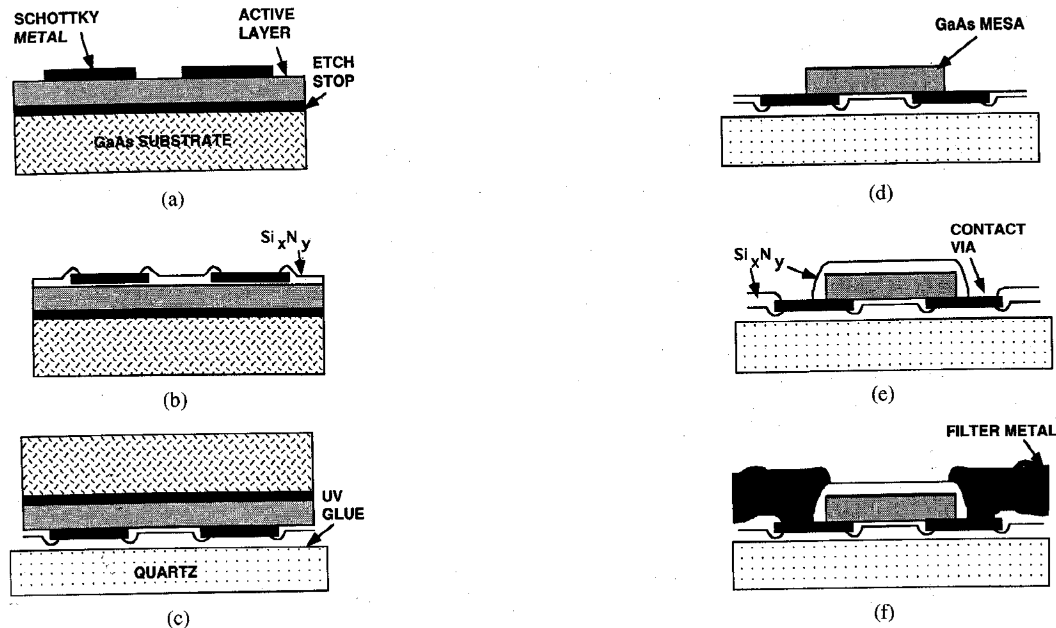


Fig. 3. The fabrication process steps for the integrated planar GaAs bbBNN varactor device. (a) MBE growth with Schottky metallization. (b) Surface passivation and dielectric window opening. (c) Mounting on quartz. (d) Lapping, etching, mesa definition, and removal of unwanted semiconductor substrate portions. (e) Backside passivation and contact vias. (f) Backside metal contacts and filter metal patterning.

In this paper the authors describe a 220-GHz tripler composed of a novel waveguide mount [4] and an integrated bbBNN device in which a new backside etch processing technique [5] has been used to remove all non-essential semiconductor material from the vicinity of the device. The bbBNN is integrated directly with much larger quartz microstrip filter circuitry to yield a more readily handled package which can scale potentially to frequencies as high as 1 THz. Measurements of the tripler performance are compared with computer simulations using a modified version of the code developed in [6] to gain a better understanding of the device limitations and potential performance realization.

II. Integrated bbBNN Device

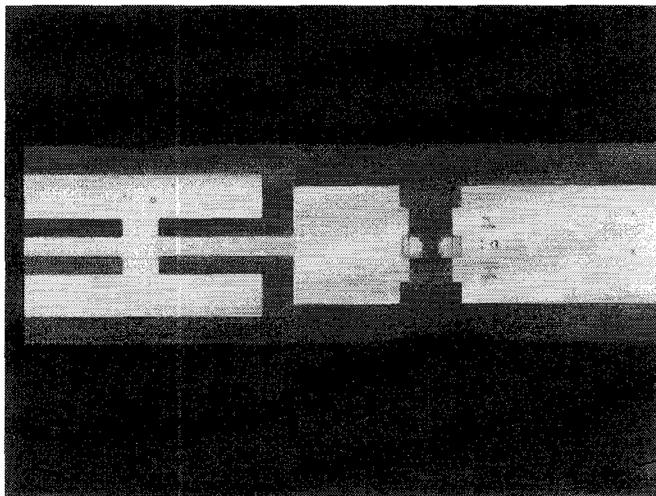
Fig. 1 shows the schematic diagram of the planar bbBNN varactor structure, integrated with a microstrip filter on a quartz substrate. The bulk of the circuit is composed of fused quartz with a patterned gold top layer. The remainder of the circuit consists of a small semiconductor mesa that forms the active bbBNN device. The device is held in position via a UV-cured adhesive in a technique first described in [7].

A cross-sectional view of the active area of the device is shown in Fig. 2. Since the structure consists of two diodes tied back-to-back by a highly doped GaAs region, the capacitance versus voltage characteristic is symmetric. The maximum capacitance occurs at zero bias, when there is a high level of induced free charge from the planar doping sheet at the bottom of the AlGaAs/GaAs interface. The minimum capacitance is obtained when a bias is applied so that one diode is in accumulation and the other is fully depleted. The resulting capacitance is the series combination of the capacitance of the two diodes, with most of the capacitance change occurring across the depleted device. The layer thicknesses, compositions and doping densities, along with the number of barrier layers and the device geometry, can be independently tailored to optimize the device for the desired frequency. Combinations of depletion layer doping and planar doping sheets allow some tailoring of the capacitance versus voltage characteristic [1].

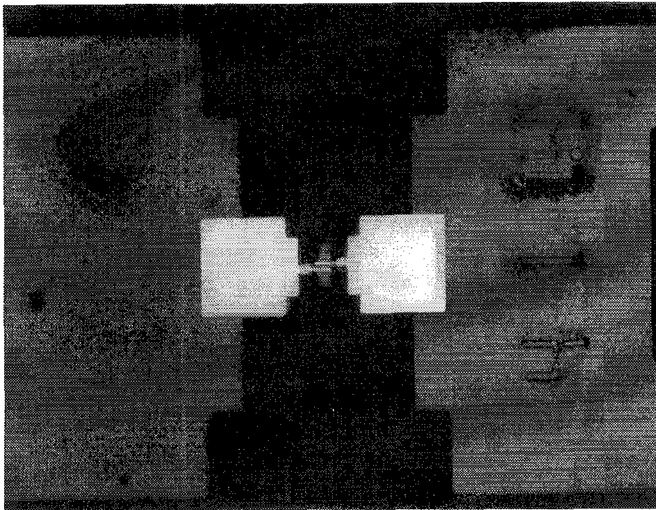
A. Fabrication of Integrated bbBNN Varactor

A fabrication process was designed to integrate the planar bbBNN device with distributed quartz microstrip filter circuitry and to eliminate all the GaAs on the final circuit structure except for the small active GaAs mesa region. It has been demonstrated that, prefabricated and thinned GaAs substrate devices can be transplanted onto quartz using UV-cured optical cement [7]. However, this process, which uses a surface channel etch to achieve diode isolation, leaves highly doped GaAs around the devices and under the distributed circuit elements, which can be detrimental to the RF performance. Other, more conventional, diode isolation techniques have a number of drawbacks. Isolation implants are commonly used, but the removal of masking materials from the wafer often present difficulties. An alternative technique for isolating active devices is to perform a mesa etch, but contacting the top of the mesa generally requires using a planarization or air bridge process. Our experiments have indicated that the planarization process damages the thin barrier layer of the BNN wafer, while an air bridge process is difficult to use on small area devices with deep mesas.

The integration process presented here uses a backside processing technique [5] in which the front of the wafer is exposed to a minimum amount of processing. The salient process steps are shown in Fig. 3. The GaAs wafer structure (Fig. 3(a)) consists of 1) a 2-nm-thick GaAs cap layer, 2) a 20-nm $Al_{0.45}Ga_{0.55}As$ barrier, 3) a 3-nm GaAs spacer followed

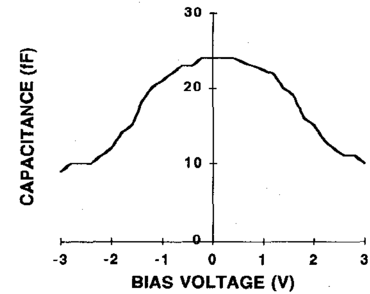


(a)

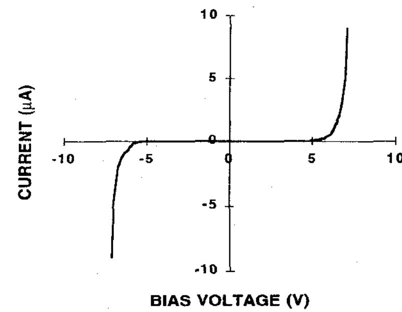


(b)

Fig. 4. (a) Photograph of a completed and diced integrated bbBNN on a gold/quartz hammerhead microstrip filter structure. (b) Close-up view of the integrated bbBNN device seen through the quartz substrate.



(a)



(b)

Fig. 5. Measured (a) C–V and (b) I–V characteristics of an 8-μm^2 integrated bbBNN varactor.

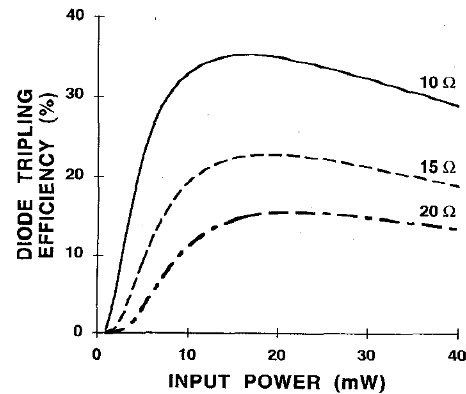


Fig. 6. Computed bbBNN tripling efficiency to 220 GHz versus input power parameterized by the device series resistance.

by 4×10^{12} cm^{-2} silicon planar doping, 4) a 120-nm-thick moderately doped GaAs layer (doping level $= 1 \times 10^{17}$ cm^{-3}), 5) a 1300-nm-thick highly doped GaAs layer (doping level $= 5 \times 10^{18}$ cm^{-3}), and 6) a 600-nm-thick $Al_{0.45}Ga_{0.55}As$ etch stop layer grown by MBE on a 500-μm-thick semi-insulating GaAs substrate.

To begin the process, Schottky contacts are defined by lift-off of e-beam evaporated Ti/Pt/Au. The wafer is then passivated with 1200 Å of ECR deposited silicon nitride. Using reactive ion etching, windows in the nitride are opened over the metal contact pads away from the active area of the device. The wafer is then bonded face down to a 0.152-mm-thick quartz substrate with a thin layer (approximately 5–10 μm) of commercially available UV curing optical adhesive (Norland type 61). The windows in the nitride allow the glue to adhere directly to the metal pads, which helps to prevent metal peeling during later probe testing and wire bonding of the devices. The quartz mounted wafer is first mechanically lapped to about 100 μm. The semiconductor substrate is further thinned in a selective etch that removes the remaining bulk GaAs, stopping on the AlGaAs etch stop layer. Mesas are patterned from the backside of the wafer using an IR mask aligner (while the backside illumination is necessary, the wafer is sufficiently thin that the IR feature is not required). A dry etch containing BCl_3, Cl_2, and Ar removes all the nonessential semiconductor material surrounding the active area, thus isolating the devices and exposing the metal contact pads. After removal of the mesa photoresist, the backside is passivated with a second layer of silicon nitride and contact windows are opened by photolithography and reactive ion etching. The backside metal contact pads, and subsequently the microstrip filter circuitry, are defined using Cr/Au evaporation and lift-off techniques. The final filter structure has 1-μm-thick evaporated gold to reduce the skin effect resistance. Fig. 4(a) shows a photograph of the integrated device. Fig. 4(b) shows a close-up view of the device portion of the integrated filter through the 0.152-mm-

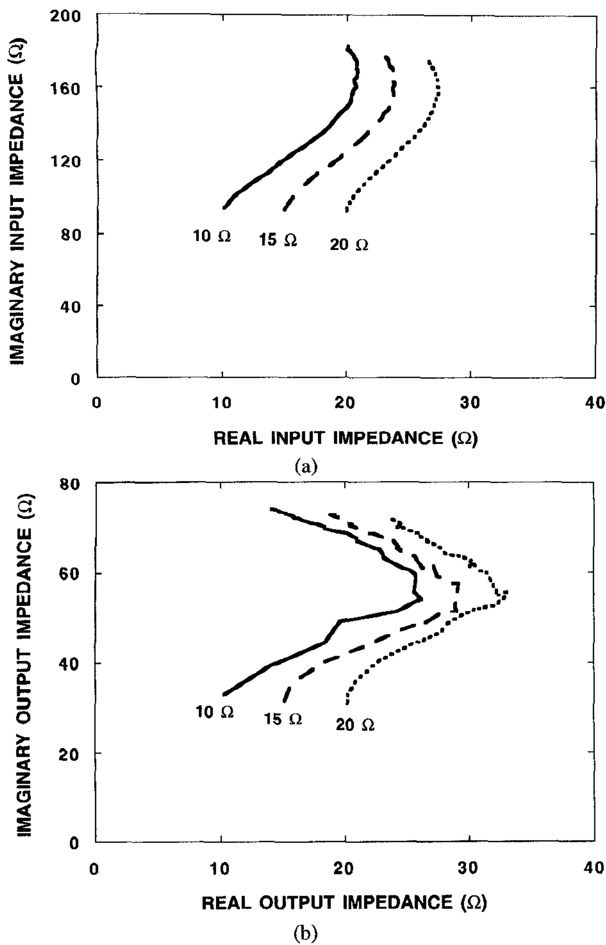


Fig. 7. Theoretical optimum embedding impedances for the integrated bbBNN varactor tripler to 220 GHz as a function of input power parameterized by device series resistance. (a) At 73.3 GHz. (b) At 220 GHz.

thick transparent quartz substrate. Two fingers at the center of this photograph define the Schottky contact area across the mesa top surface, and connect the device to the contact pads.

B. dc Device Characteristics

A mask set containing many device and circuit variations was generated. The design parameters for the devices were obtained using the procedures outlined in [8]. The integrated devices which gave the best performance in these experiments have an area of 8 μm^2, a GaAs mesa width of 4 μm and metal contact fingers which are 2 μm wide and separated by a 1.4-μm gap. The chosen design parameters of the devices are: maximum capacitance, $C_{\max} = 23$ fF, capacitance ratio, $C_{\max}/C_{\min} = 4$, dc series resistance, $R_s = 11$ Ω, breakdown voltage, $V_{br} = 22$ V, dynamic cut-off frequency, $f_{cd} = 1/(2\pi R_s C_{\min})\{1 - C_{\min}/C_{\max}\} = 1.9$ THz. R_s comes mainly from the n$^+$ region and to a lesser extent from the sheet doping and depletion layers [8]. Unlike a typical Schottky varactor, the series resistance is not necessarily affected by changes which alter the $C_{\max}/C\text{min}$ ratio and therefore need not be traded off with doping in realizing higher cut-off frequencies [8].

Typical measured dc characteristics for the 8-μm^2 device, which gave the best performance are: $C_{\max} = 24$ fF, $C_{\max}/C_{\min} = 2.7$, and $V_{br} = 6$ V. R_s cannot be measured at dc, however, equivalent circuit modeling of similar devices had values between 11 and 14 Ω when measured on a special test fixture at 1–20 GHz [3]. Fig. 5 shows the current–voltage (I–V) and 1 MHz capacitance–voltage (C–V) characteristics of a typical 8-μm^2 device on the quartz RF microstrip filter circuitry. The disparity between the predicted and measured $C_{\max}/C_{\min}$ ratio is most likely due to unmodeled parasitic capacitances which raise the value of $C_{\min}$. The lower than expected breakdown voltage may be due to avalanching and edge effects.

III. Computed Tripler Performance

The performance of the 8-μm^2 bbBNN device described in this paper has been calculated using a modified version of the large signal analysis program [6]. The program has been modified to handle the measured C–V and I–V characteristics of the bbBNN varactors (shown in Fig. 5), including a frequency dependent series resistance. The input and output embedding impedances are optimized for best computed tripling efficiency. Harmonic frequencies other than the output are short circuited.

Since the series resistance of the bbBNN is an important parameter but is not readily derived from dc measurements, the calculations are carried out for a range of values (corresponding to a range of cut-off frequencies). Fig. 6 presents the computed diode tripling efficiency versus input power for the integrated bbBNN varactor used in this experiment plotted for series resistance values of 10, 15, and 20 Ω. Higher device series resistances degrade the performance significantly.

Optimized embedding impedances for an input frequency of 73.3 GHz and a third harmonic frequency of 220 GHz were computed with input power levels up to 40 mW. The resulting curves are shown in Fig. 7, again as a function of series resistance. At low input power, the real part of the impedance is the same as the diode series resistance and the imaginary part of the impedance is 90 Ω at the input frequency and 30 Ω at the output frequency, corresponding roughly to zero bias capacitance. The pumped capacitance decreases with increasing input power, thereby increasing the imaginary part of the embedding impedance. The minimum capacitance of 9 fF corresponds to 220 Ω at the input frequency and 80 Ω at the output frequency. As can be seen in the plots, for optimum performance, the waveguide mount must match real impedances in the range 10–30 Ω at the input and output frequencies. The imaginary impedances needed are in the range from 90–200 Ω for the input circuit and from 30–75 Ω for the output circuit.

IV. Waveguide Mount Description

A split-waveguide mount was used to provide the desired input and output embedding impedances to the integrated bbBNN device. This mount has been described elsewhere [4]. Modifications used especially for the bbBNN devices described here include: separate tuning stubs at the input and output frequencies, which lie in microstrip channels beyond the output waveguide wall, a channel waveguide transformer [9], which increases both the height and width (slightly) of the

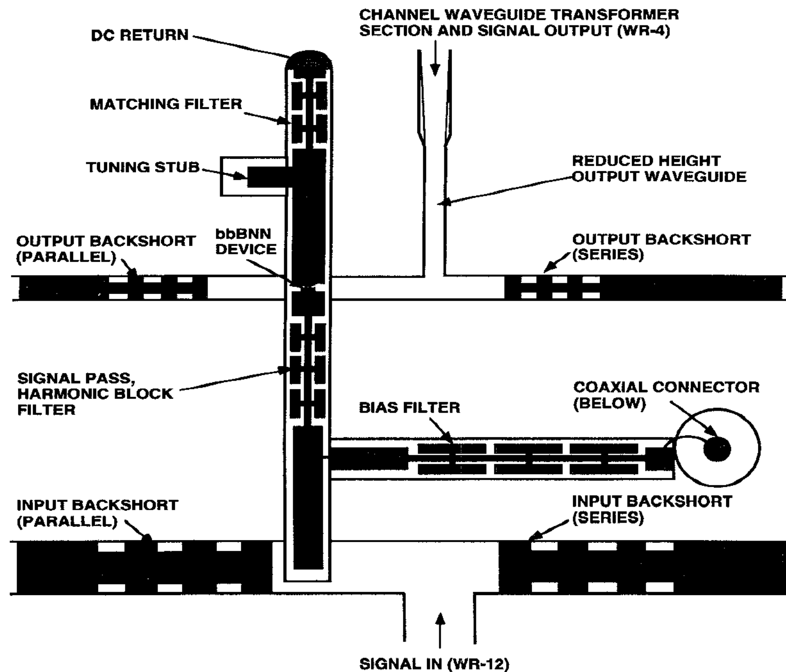


Fig. 8. Close-up view of the filter portion of the 220-GHz tripler mount.

output waveguide, and noncontacting backshorts [10] in both the series and parallel tuning arms of the input and output waveguides. The bbBNN device is positioned at the center of the broad wall of the output waveguide (half height WR-4 waveguide –0.28 mm × 1.09 mm). The distances of the input and output E-plane waveguides from the microstrip filter are approximately $\lambda_{\text{guide}}/2$ at the fundamental and third harmonic frequencies, respectively. The microstrip filter channel is 0.36 mm wide and 0.31 mm high and it extends across and beyond the output tuner waveguide (where the matching stubs lie). A dc return is supplied by a wire bond at the end of the microstrip filter. Bias voltage can be applied to the device (to check characteristics, for instance) through a pump-block filter and SMA connector which are contained in the lower half of the tripler block (see Fig. 8).

The integrated RF filter and the bias filter (see Fig. 8) help to achieve both signal separation and matching. These microstrip hammerhead filters are fabricated on 0.33-mm-wide and 0.152-mm-thick fused quartz substrates. Fine tuning of the filter response was accomplished using the finite difference time domain (FDTD) method [11]. The bias filter rejects the 60–80 GHz input power. The RF filter passes the input frequency, but rejects the tripled output power. The filter on the far side of the output tuner waveguide presents a short circuit at the waveguide wall at the third harmonic frequency and presents a reactive termination, via a side stub, at the fundamental frequency.

V. RF Performance

The tripler performance was measured using the technique described in [12]. Gunn oscillators were used as pump sources and no device bias was applied during the measurements. The tripling efficiency of the bbBNN device refers to Anritsu type TC power meter heads at the input and output waveguide flanges. The reflected power is monitored during measurement using a directional coupler and a third power meter.

Measurements were carried out over the frequency range of 200–240 GHz. The best performance was achieved at an output frequency of 217.5 GHz. Fig. 9(a) shows the measured tripling efficiency versus input power for the 8-μm^2 integrated bbBNN varactor in the split-waveguide mount. The efficiency of the tripler reaches its maximum value of 7% at 8.8 mW input power and then begins to decrease as the pump power level is increased. Fig. 9(b) shows the tripled output power versus input power for this device. A maximum output power of about 730 μW was measured for 14.3 mW input power. Fig. 9(c) presents the tripling efficiency versus output frequency curves for different input power levels. Input impedance matching was easily obtained for these measurements, but output impedance matching was difficult and changed rapidly with slight variation of input frequency and power levels.

Many other bbBNN devices with varying values of zero bias capacitances were measured in this waveguide block, but none performed as well as the 8-μm^2 device. The tripling efficiency was found to depend greatly, as expected, on the $C_{\text{max}}/C_{\text{min}}$ ratio and this ratio varied significantly from device to device. Subsequent model measurements on scaled bbBNN's at 10 GHz [13] showed very similar trends.

VI. Conclusion

The performance of a monolithically integrated planar bbBNN varactor tripler has been presented. A device development process has been described which integrates the bbBNN with a larger tuning circuit on a quartz substrate. The resulting planar structure is scaleable to submillimeter wave frequencies and allows for significantly more flexibility in circuit design than would be available with a whisker contacted or discrete varactor chip technology.

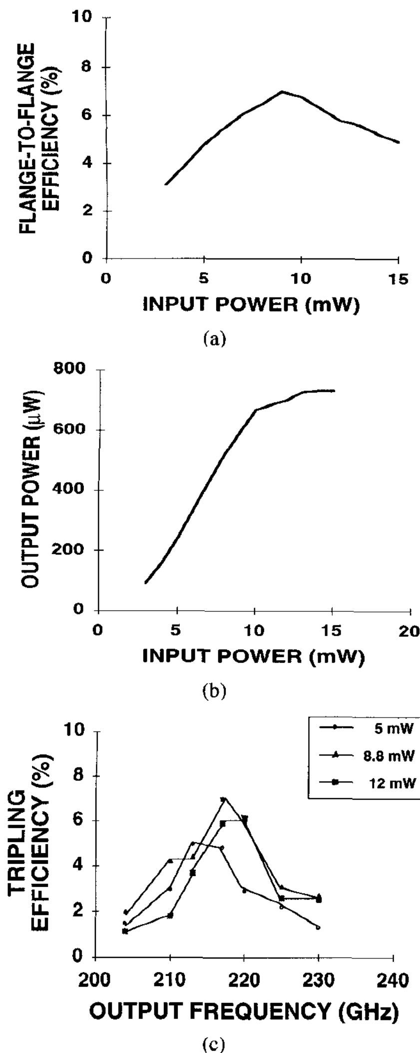


Fig. 9. (a) Measured tripling efficiency versus input power for the 8-μm^2 bbBNN device at 217.5 GHz. (b) Measured output power versus input power for the same device at 217.5 GHz. (c) Measured tripling efficiency versus output frequency at input power levels of 5, 8.8, and 12 mW.

A flange-to-flange tripling efficiency of 7% and a maximum output power of about 730 μW were measured for the integrated bbBNN device. Although this efficiency is higher than previously reported for a planar device structure, it is much less than expected from the computer simulations, and the differences cannot be attributed solely to circuit losses. The reasons for the discrepancy are not understood, however there is some recent work [14] which indicates that the large signal analysis used for our computer simulations significantly over estimates the conversion efficiency for the bbBNN as well as other heterostructure devices. The predicted shape of the power versus efficiency curves and the input power at which the highest tripling efficiency occurs do, however, agree with those measured at 220 GHz even if the absolute levels are much lower. A similar trend is seen on a 10-GHz scale model of the tripler block with scaled bbBNN structures.

Finally, the best devices used in this study have a C_{max}/C_{min} of 2.7 or less. Increasing the C_{max}/C_{min} ratio should significantly improve the performance of the bbBNN without significantly decreasing the dynamic cut-off frequency [8]. The C_{max}/C_{min} ratio can be improved by proper optimization of the doped and sheet charge layer structures and by reducing the parasitic capacitances associated with the device structure. Any increase in C_{max}/C_{min} will translate into higher potential conversion efficiencies and higher achievable operating frequencies. To date, single whisker-contacted Schottky varactor triplers and planar Schottky varactor doublers have conversion efficiencies which exceed 20% [15], [16]. However, the bbBNN device has only been available for a relatively short time, and because of its very versatile structure, only a small set of the available parameter space has been explored. Its natural potential for odd harmonic generation, easily realizable planar structure and versatile composition make it a device of considerable interest. With additional experimental work, improvement in performance seems likely in the future.

ACKNOWLEDGMENT

The authors would like to express their special thanks to A. Pease and M. Natzic for their help in mounting the integrated device structures in the split-waveguide mounts and John Oswald for the analysis of the hammerhead filter structures.

REFERENCES

[1] M. A. Frerking and J. R. East, "Novel heterojunction varactors," *Proc. IEEE*, vol. 80, pp. 1853–1860, Nov. 1992.

[2] U. Lieneweg, T. J. Tolmunen, M. A. Frerking, and J. Maserjian, "Modeling of planar varactor frequency multiplier devices with blocking barriers," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 839–845, May 1992.

[3] D. Choudhury, A. V. Räisänen, R. P. Smith, M. A. Frerking, S. C. Martin, and J. K. Liu, "Experimental performance of a back-to-back barrier-N-N+ (bbBNN) varactor tripler at 200 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 755–758, Apr. 1994.

[4] A. V. Räisänen, D. Choudhury, R. J. Dengler, J. E. Oswald, and P. H. Siegel, "A novel split-waveguide mount design for millimeter- and submillimeter-wave frequency multipliers and harmonic mixers," *IEEE Microwave and Guided Wave Lett.*, vol. 3, pp. 369–371, Oct. 1993.

[5] R. P. Smith, D. Choudhury, S. C. Martin, M. A. Frerking, J. K. Liu, and F. A. Grunthaner, "A new fabrication technique for back-to-back varactor diodes," in *Proc. Third Int. Symp. Space Terahertz Technol.*, 1992, pp. 158–163.

[6] P. H. Siegel, A. R. Kerr, and W. Hwang, "Topics in the optimization of millimeter wave mixers," NASA Tech. Paper 2287, 1984.

[7] W. L. Bishop, E. R. Meiburg, R. J. Mattauch, T. W. Crowe, and L. Poli, "A micron thickness, planar Schottky diode chip for THz applications with theoretical minimum parasitic capacitance," in *1990 IEEE Int. Microwave Symp. Dig.*, 1990, pp. 1305–1308.

[8] D. Choudhury, A. V. Räisänen, R. P. Smith, and M. A. Frerking, "Study of the effect of the C_{max}/C_{min} ratio on the performance of back-to-back barrier-N-N+ (bbBNN) varactors for frequency multiplier applications," *IEEE Microwave and Guided Wave Lett.*, vol. 4, pp. 101–103, Apr. 1994.

[9] P. H. Siegel, D. W. Peterson, and A. R. Kerr, "Design and analysis of channel waveguide transformer," *IEEE Trans. Microwave Theory Tech.*, vol. 31, pp. 473–484, June 1983.

[10] M. K. Brewer and A.V. Räisänen, "Dual-harmonic non-contacting millimeter waveguide backshort: Theory, design and test," *IEEE Trans. Microwave Theory Tech.*, vol. 30, pp. 708–714, May 1982.

[11] J. E. Oswald and P. H. Siegel, "The application of the FDTD method to millimeter-wave filter circuits including the design and analysis of a compact coplanar strip filter for THz frequencies," in *1994 IEEE Microwave Theory Tech. Symp. Dig.*, San Diego, CA, May 1994, pp. 309–312.

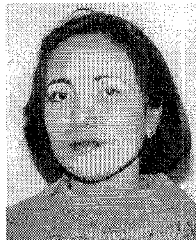
[12] D. Choudhury, M. A. Frerking, and P. D. Batelaan, "A 200-GHz tripler using a single barrier varactor," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 595–599, Apr. 1993.

[13] P. H. Siegel, unpublished data.

[14] S. R. Jones, University of Virginia, private communication.

[15] N. R. Erickson, "A high efficiency frequency tripler for 230 GHz," in *Proc. 12th Eur. Microwave Conf.*, Helsinki, Finland, Sept. 1982, pp. 288–292.

[16] B. J. Rizzi, T. W. Crowe, and N. R. Erickson, "A high-power millimeter-wave frequency doubler using a planar diode array," *IEEE Microwave and Guided Wave Lett.*, vol. 3, pp. 188–190, June 1993.



Debabani Choudhury (M'91) received the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 1991.

In July 1991, she joined the Advanced Devices group of NASA's Jet Propulsion Laboratory, California Institute of Technology, as a post-doctoral research associate. She was involved in all aspects of the submillimeter wave solid-state local oscillator development effort at JPL, for astrophysics and Earth remote sensing applications. She joined the Submillimeter Wave Advanced Technology group at JPL in January 1993. There, she was responsible for the development of planar varactor frequency multipliers. She joined Millitech Corporation in August 1994. As a senior member of the technical staff at the Advanced Technology Center of Millitech, she is involved in the development of wave processing semiconductor integrated circuits for imaging systems. She is also working on the design and development of multiplier circuits and other millimeter- and submillimeter-wave components. Her current research interests include micrometer- , millimeter- , and submillimeter-wave components and subsystems, design and development of semiconductor devices, computer-aided analysis and design, MMIC's, and quasi-optical techniques.

Dr. Choudhury is the recipient of NASA Certificate of Recognition Awards for her work on planar varactor devices and multiplier circuits. In 1994 she received NASA's distinguished Group Achievement Award for Submillimeter Sensors Team.

Peter H. Siegel (M'75) graduated from Colgate University, Hamilton, NY, in January 1976 and received the M.S. and Ph.D. degrees in electrical engineering from Columbia University, NY, in 1978 and 1983, respectively.

From 1975 to 1983, he worked on millimeter-wave components at the NASA Goddard Space Flight Center, Institute for Space Studies, NY, under Dr. A. R. Kerr. Following a one-year fellowship with the National Research Council, he went to work in Charlottesville, VA, at the National Radio Astronomy Observatory under Dr. S. Weinreb, where he was responsible for maintaining and developing millimeter-wave mixers for the Kitt Peak 12-m radio telescope. In 1987, he joined the Advanced Devices group under Dr. M. A. Frerking, at the California Institute of Technology Jet Propulsion Laboratory. He later formed, and currently supervises, the Submillimeter Wave Advanced Technology team, which provides both research and development as well as instrumentation support for NASA's advanced submillimeter-wave missions. His research interests include millimeter- and submillimeter-wave devices and subsystems. He is a co-investigator on the Earth Observing System Microwave Limb Sounder instrument under Dr. J. Waters, in charge of developing the millimeter- and submillimeter-wave heterodyne front ends, as well as working on advanced local oscillator development and superconducting receiver technology for submillimeter-wave astrophysics applications.

R. Peter Smith received the B.Sc. degree in physics from Bates College, Lewiston, ME, in 1977 and the M.Sc. and Ph.D. degrees from Brown University, Providence, RI, in 1982 and 1986, respectively.

From 1986 to 1990, he worked at the GE Electronics Laboratory, Syracuse, NY, and is currently employed at the California Institute of Technology Jet Propulsion Laboratory, Pasadena, CA. His research interests currently include a number of high-speed electronic devices and related circuits. He is working on grid amplifiers using HEMT's, the development of RTD's and grid oscillators using RTD's, and a number of other GaAs-based diode structures, including varactors, microwave rectifiers, and mixers.

Antti V. Räisänen (S'76–M'81–SM'85–F'94) received the Diploma Engineer (M.Sc.), the Licentiate of Technology, and the Doctor of Technology degrees in electrical engineering from the Helsinki University of Technology (HUT), Espoo, Finland, in 1973, 1976, and 1981, respectively.

From 1973 to 1978, he worked as a research assistant at the HUT Radio Laboratory. From 1978 to 1979, he was a research assistant at the Five College Radio Astronomy Observatory (FCRAO) of the University of Massachusetts, Amherst. From 1980 to 1983, he was a research fellow of the Academy of Finland, working mainly at HUT, but also for shorter periods at FCRAO and the Chalmers University of Technology, Gothenburg, Sweden. In 1984, he was a visiting scientist at the Department of Physics of the University of California, Berkeley. From 1985 to 1989 he was an acting professor of radio engineering with HUT, working also for short periods at the University of California, Berkeley. In 1989, he was appointed by invitation to the Professor Chair of Radio Engineering with HUT. In 1992–1993 he was on sabbatical leave with HUT and had a senior research fellowship from the National Research Council at the Jet Propulsion Laboratory, Pasadena, CA. He was also a visiting associate in electrical engineering at the California Institute of Technology. He is supervising research in millimeter components, antennas and receivers, microwave propagation in satellite links, microwave measurements, etc. at HUT Radio Laboratory. He has authored and co-authored more than 200 scientific or technical papers and three books: *Microwave Measurement Techniques, Radio Engineering,* and *RF and Microwave Techniques* (in Finnish).

Dr. Räisänen was the Secretary of the 12th European Microwave Conference, 1982. He was the Counselor of the IEEE Student Branch in Helsinki from 1982 to 1989, and the Chairman of the IEEE MTT/AP Chapter in Finland from 1987 to 1992. In 1992, he served as the Conference Chairman for the 22nd European Microwave Conference.

Suzanne C. Martin received the B.S. and M.S. degrees in electrical engineering from Brown University, Providence, RI, in 1985 and 1991, respectively.

From 1985 to 1989, she worked as a research engineer at Brown University designing and fabricating germanium photodiodes and MOSFET's. She is currently a member of the technical staff at the Jet Propulsion Laboratory, and is involved in the fabrication of HEMT's, RTD's, and varactor diodes for submillimeter-wave applications in addition to work on germanium gamma-ray detectors for astrophysics applications

Margaret A. Frerking (M'83) received the Ph.D. degree in physics from the Massachusetts Institute of Technology, Cambridge, MA, in 1977.

She is currently Assistant Section Manager for the Microwave Observation Systems Section of the Jet Propulsion Laboratory, California Institute of Technology, and Technologist for the Submillimeter Wave Sensors Program. She has over 15 years of experience in observational and experimental astrophysics and Earth remote sensing. As a graduate student at MIT, she developed a 9.6-μm heterodyne receiver that was used for observations of ozone in terrestrial atmosphere. She then spent three years at AT&T Bell Laboratories as a post doctoral fellow in the Radio Astronomy group studying protostellar star formation in dark molecular clouds. She joined the JPL staff in 1980 and became the cognizant engineer for the development of the 205-Ghz radiometer for the Microwave Limb Sounder on the Upper Atmospheric Research Satellite. She was also a member of the JPL team responsible for the KAO vapor radiometers that operated at 183, 380, and 546 GHz. In 1986, she became the Technical Group Supervisor of the submillimeter development group. In 1993, she attained her current position, which includes research to develop submillimeter SIS mixers, solid-state local oscillator sources, and heterodyne receiver array techniques. She has published more than 75 papers.

Dr. Frerking is a member of the American Astronomical Society, Sigma Xi, Phi Beta Kappa, and the the NASA OSSA Submillimeter Working Group.